**USB & TRNG ATE Test Plan**

Revision history

|  |  |  |  |
| --- | --- | --- | --- |
| Revision | Date | Description | Author |
| 0.1 | 2017-09-13 | Initial | Hao Sun |
| 0.2 | 2017-09-28 | Add Needed device list for USB | Hao Sun |
|  |  |  |  |

## USB

### Methodology

The DWC USB 3.0 PHY IP was designed with ATE testing in mind. Features were added inside the IP to aid the testing process. Tests were developed early on in development to ensure sufficient test coverage of blocks inside the IP, and external requirements were kept to a minimum. All that is needed on a load board is a simple AC-coupled serial loopback for the DWC USB 3.0 PHY, a reference clock, and a 200ohm resistor.

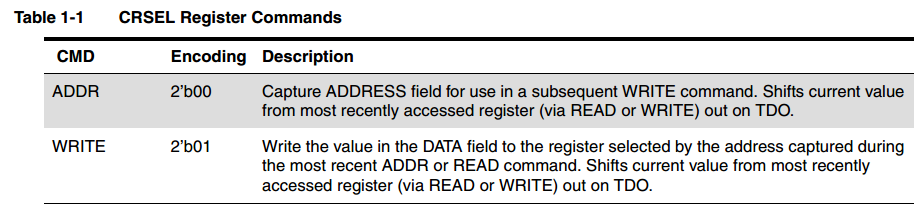
Typically, each test is configured through the JTAG port by writing internal IP registers. A measurement is then made and compared against limits, and a pass/fail value is returned through the JTAG port. The limits are embedded inside the JTAG vector to account for variations between load boards or ASIC implementations. In the Synopsys solution, no vector capture is required. Every test returns a simple pass/fail result.

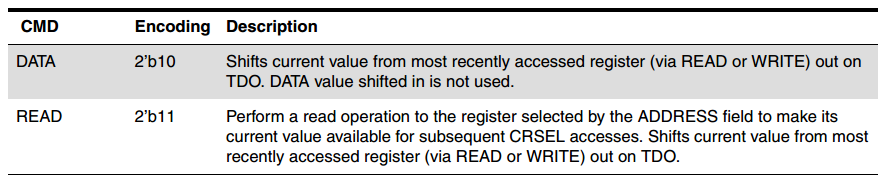
### JTAG Accessibility

Two JTAG registers, CRSEL and CRALU, are used to read, write, and manipulate control register values  
that are embedded in the analog and digital portions of the design.

**CRSEL Register**

Control register access is performed by shifting a command and either register address or data into the  
CRSEL register. The CMD field determines what type of access will be performed. Table 1-1 describes the  
encodings defined for the CRSEL.CMD field. All actions are initiated during the UPDATE-DR phase of the  
JTAG state machine while the CRSEL register is being accessed.

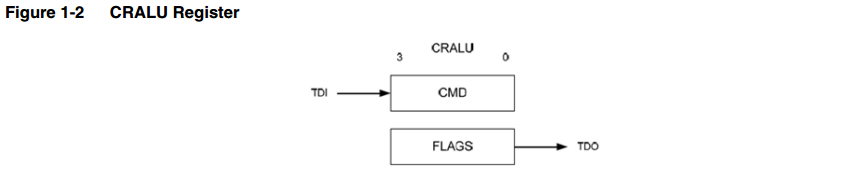




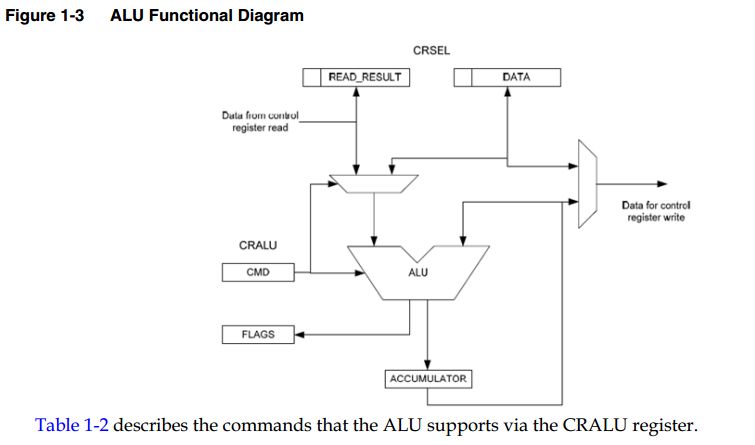
To perform a control register read, simply shift a READ command into the CRSEL register along with the register address in the ADDRESS field. Any subsequent CRSEL access will cause the data returned by the READ command to be shifted out of TDO. This action enables a limited form of pipelining READ commands, because the second access can be shifting in the command and address for the subsequent READ command while shifting out the data from the previous READ command. To perform a control register write, the ADDRESS of the register to be written must first be selected by performing either a ADDR or READ command and specifying the register address in the ADDRESS field. A second access using the WRITE command and specifying the data to be written in the DATA field will cause the write to finally be performed in the target register.

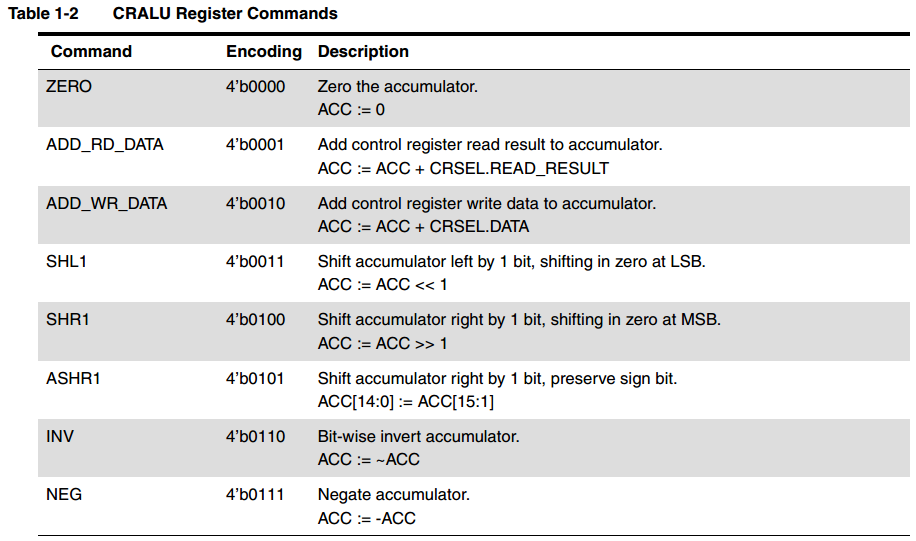
**CRALU Register**

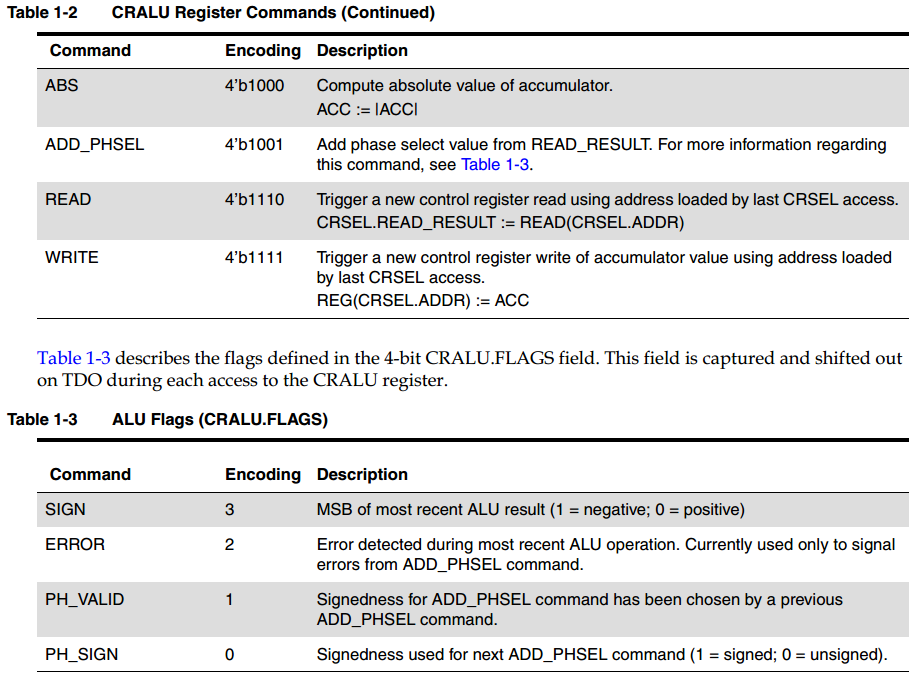
This register is a 4-bit command register that enables values from internal control registers as well as usersupplied values from the CRSEL DATA field to be manipulated using simple arithmetic operations. Figure 1-2 shows the format of the CRALU register.



An ALU with an associated 16-bit accumulator is controlled by commands written to this register, and the results can be stored back in the PHY’s control registers. Figure 1-3 shows the data and control flow between the ALU, the CRSEL register, and the CRALU register.

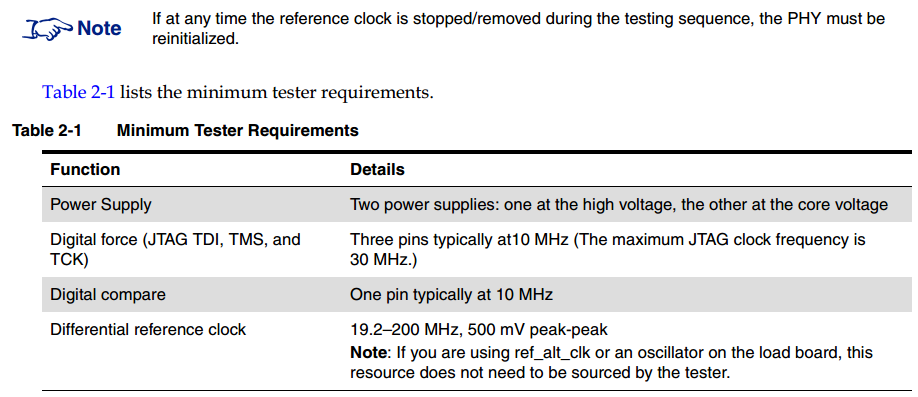






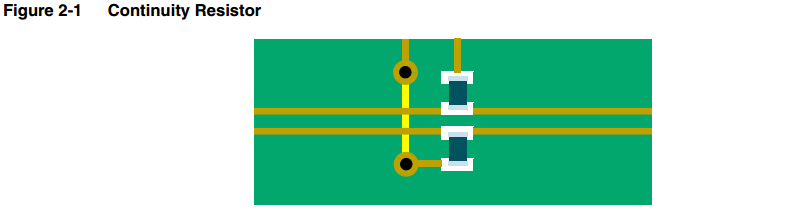
### Tester Requirements

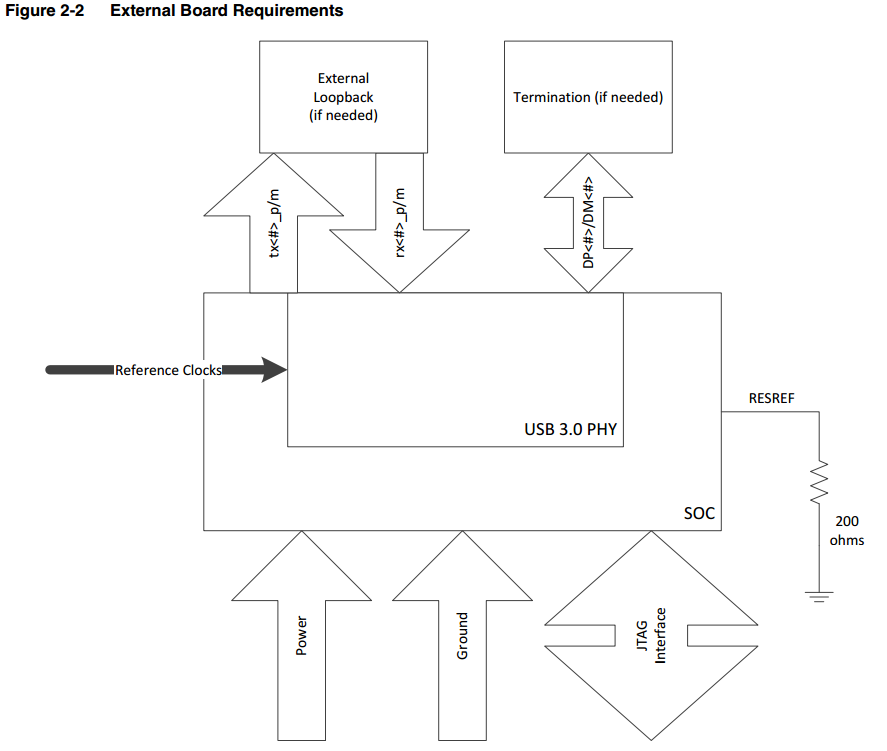
The DWC USB 3.0 PHY test methodology was developed to use minimal tester resources. The tester’s hardware requirements include two power supplies, four digital pins, and a differential reference clock. In most applications, two digital tester pins can be used as the reference clock source. The reference clock must be present before the PHY is released from reset.

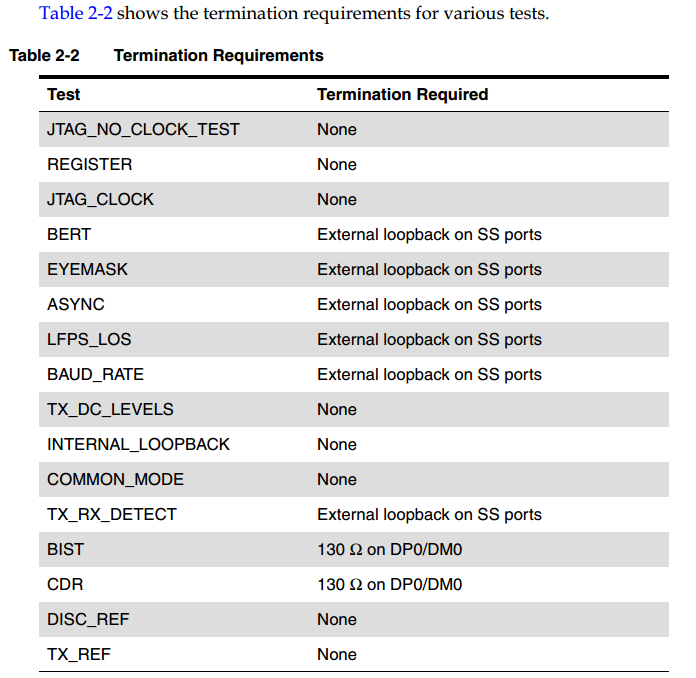


### Load Board Requirements

Load board requirements are minimal. The DWC USB 3.0 PHY requires an external 200-Ω (-1%,+1%)resistor on the resref pin. To take advantage of the built-in test capabilities, an external AC-coupled(75~200nF) loopback between the DWC USB 3.0 PHY’s transmit and receive pins is required. If continuity/leakage measurements are required on the High-Speed (HS) function’s and/or SS function’s serial interfaces, place an optional relay on the signal path. To minimize any discontinuities in the signal path, take care when placing the relay. If only a continuity check is required, you can place a high-value resistor on the SS function’s loopback path. Figure 2-1 shows the recommended layout.







### Needed device List

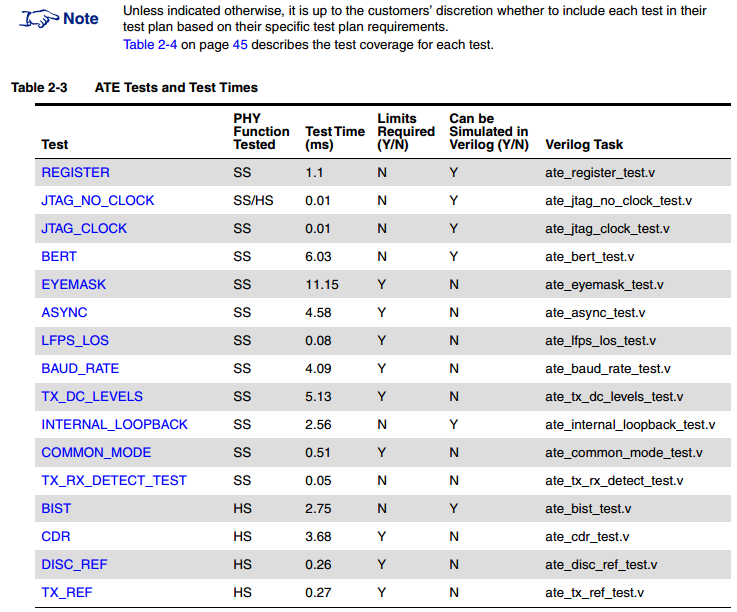
|  |  |
| --- | --- |
| **PAD name** | **value** |
| resref resistor | 200-Ω (-1%,+1%) |
| 3.0 loopback AC-coupled cap | 75~200nF |
| 2.0 termination on DP0/DM0 | 130-Ω |
| Continuity resistor on 3.0 | 10K |
|  |  |

### Pad list

|  |  |
| --- | --- |
| device name | Signal name |
| SPI\_MS3\_DI | SPI\_DBG\_DI |
| SPI\_MS3\_DO | SPI\_DBG\_DO |
| SPI\_MS3\_SCLK | SPI\_DBG\_SCLK |
| SPI\_MS3\_CS0N | SPI\_DBG\_CSN |
| SPI\_M2\_DI | TEST\_JTAG\_TDI |
| SPI\_M2\_DO | TEST\_JTAG\_TDO |
| SPI\_M2\_SCLK | TEST\_JTAG\_TCK |
| SPI\_M2\_CS0N | TEST\_JTAG\_TMS |
| USB\_RESREF | USB\_RESREF |
| USB\_RX0N | USB\_RX0N |
| USB\_RX0P | USB\_RX0P |
| USB\_TX0N | USB\_TX0N |
| USB\_TX0P | USB\_TX0P |
| USB\_DN | USB\_DN |
| USB\_DP | USB\_DP |

### ATE Test Suite

Table 2-3 lists the ATE tests and their test times (assuming a 10-MHz JTAG clock frequency). Tests that  
require limits to be set are also indicated.



#### BIST

**External Loopback Required**: N (130-Ω termination required)

**Wafer Sort:** N

This test is highly recommended, because it exercises the HS/FS and LS portions in the HS function of the DWC USB 3.0 PHY.

This test uses the BIST feature of the PHY’s HS function. This test runs BIST in HS, FS, and LS modes.

#### BERT

**External Loopback Required**: Y  
**Wafer Sort**: N  
It is highly recommended that you include this test, because it exercises the entire SuperSpeed data path. The BERT test checks the following in the SS function:

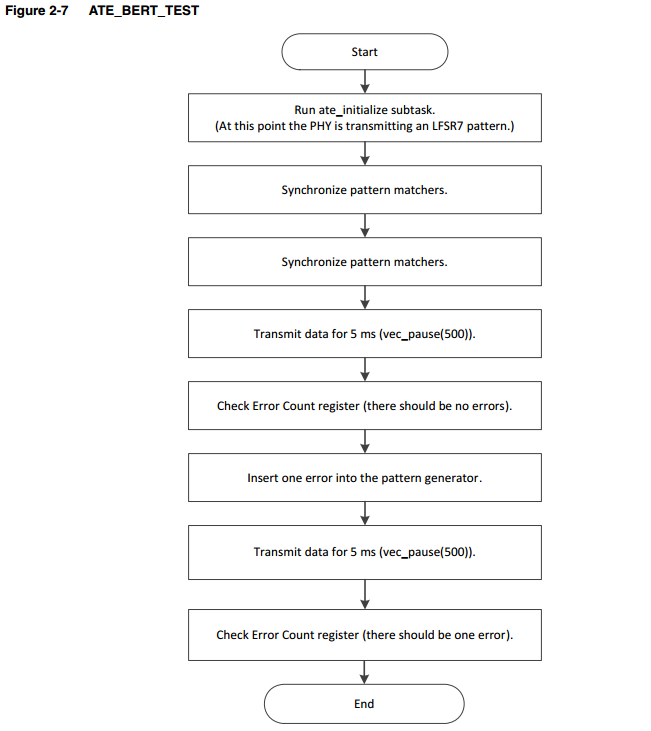
■ Signal path

■ Pattern matchers

■ Pattern generators

■ Error counters to be used in subsequent tests

This test uses an external loopback.A known LFSR7 pattern (default) is transmitted and matched at the receiver to verify that data can be passed from the transmitter to the receiver.



#### INTERNAL\_LOOPBACK

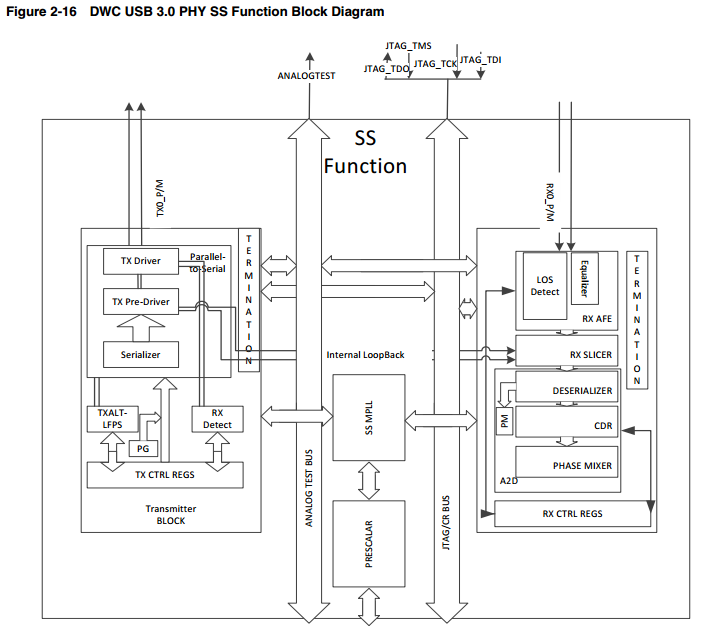
**External Loopback Required**: N

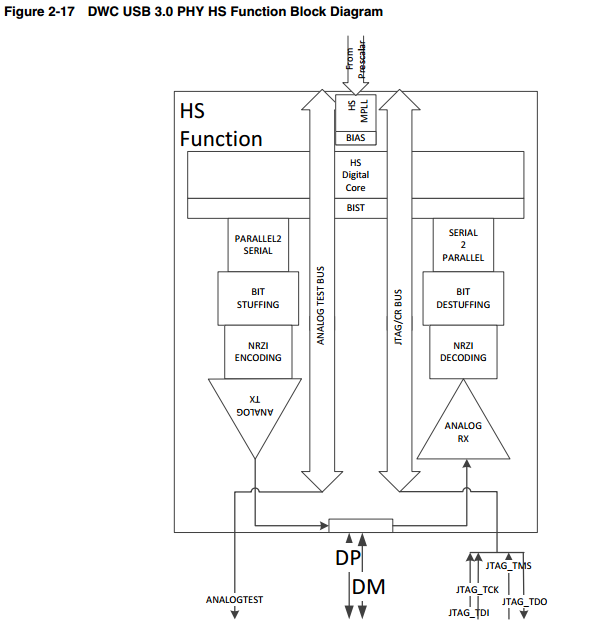
**Wafer Sort:** Y

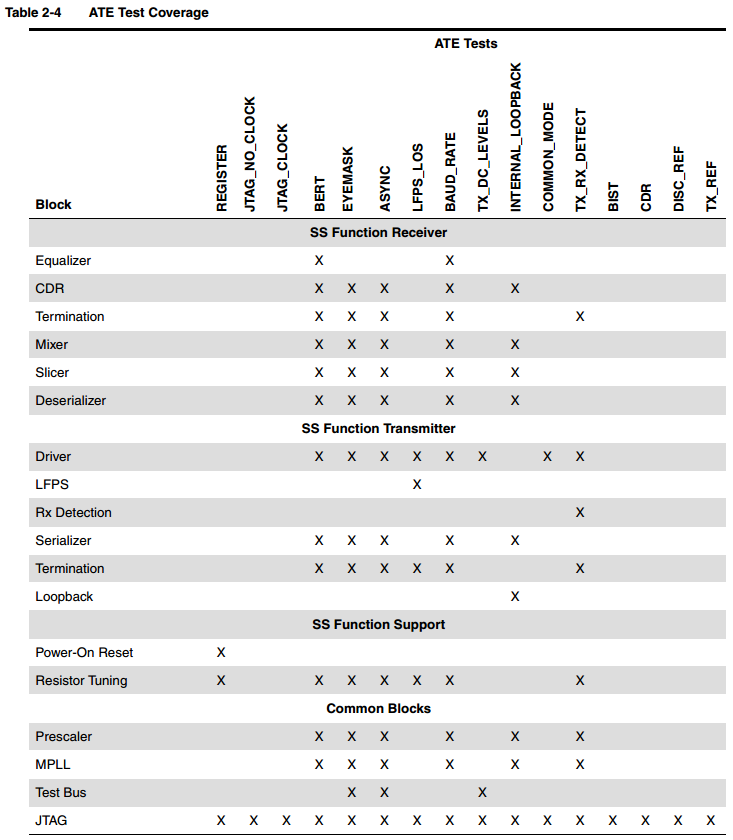
This test verifies the function of the DWC USB 3.0 PHY’s Tx-to-Rx digital serial loopback. This test is identical to the BERT/External Loopback test, except that the Rx AFE is not exercised. An internal loopback path is exercised, bypassing the Tx drivers and the Rx AFE. If BERT is being run, INTERNAL\_LOOPBACK does not have to be run at board level; instead, this test can be run before packaging at wafer sort.

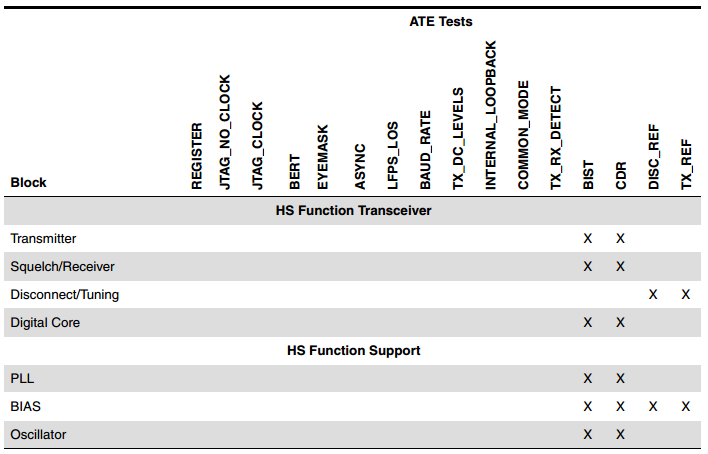
### ATE Test Coverage

Figure 2-16 and Figure 2-17 on page 44 show a block diagram of the DWC USB 3.0 PHY macro, and Table 2-4 on page 45 lists the individual tests and corresponding blocks that are exercised during the test.

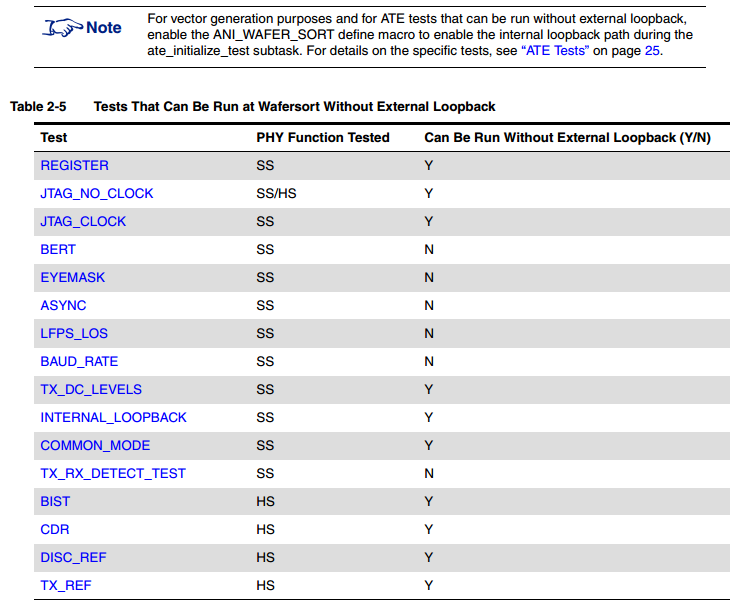






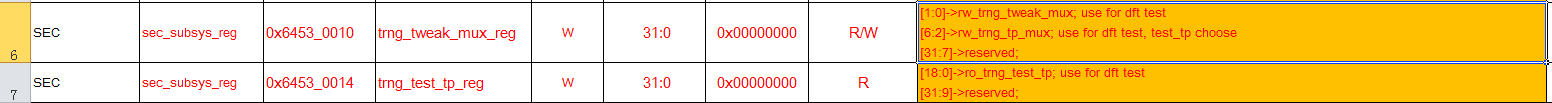


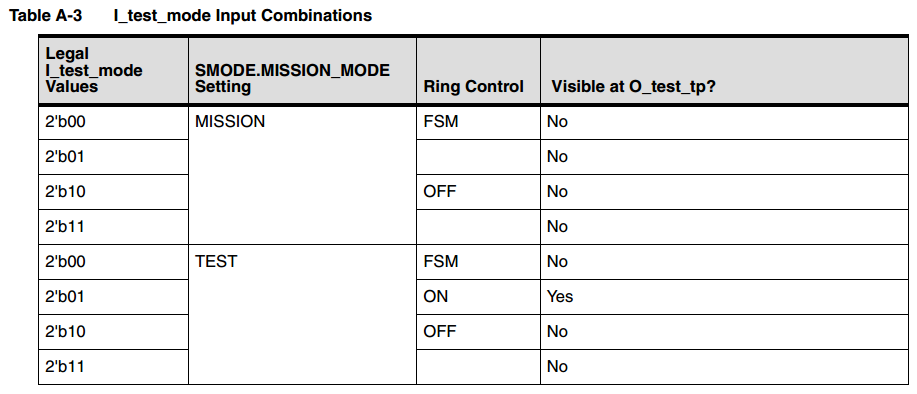
Some tests rely on the presence of external loopback from the SS transmitter to the SS receiver with the appropriate AC-coupling capacitors in order to function. At wafersort, the use of probes that can operate at multi-Gbps speeds can be costly. Table 2-5 lists each test and indicates whether the test can be run with/without external loopback on the SuperSpeed lines.



## TRNG

### Register in use





### Pad List

|  |  |
| --- | --- |
| PAD name | Signal name |
| SPI\_MS3\_DI | SPI\_DBG\_DI |
| SPI\_MS3\_DO | SPI\_DBG\_DO |
| SPI\_MS3\_SCLK | SPI\_DBG\_SCLK |
| SPI\_MS3\_CS0N | SPI\_DBG\_CSN |
| QE1\_5 | ATE\_TEST\_OUT\_9 |

### Test Logic

